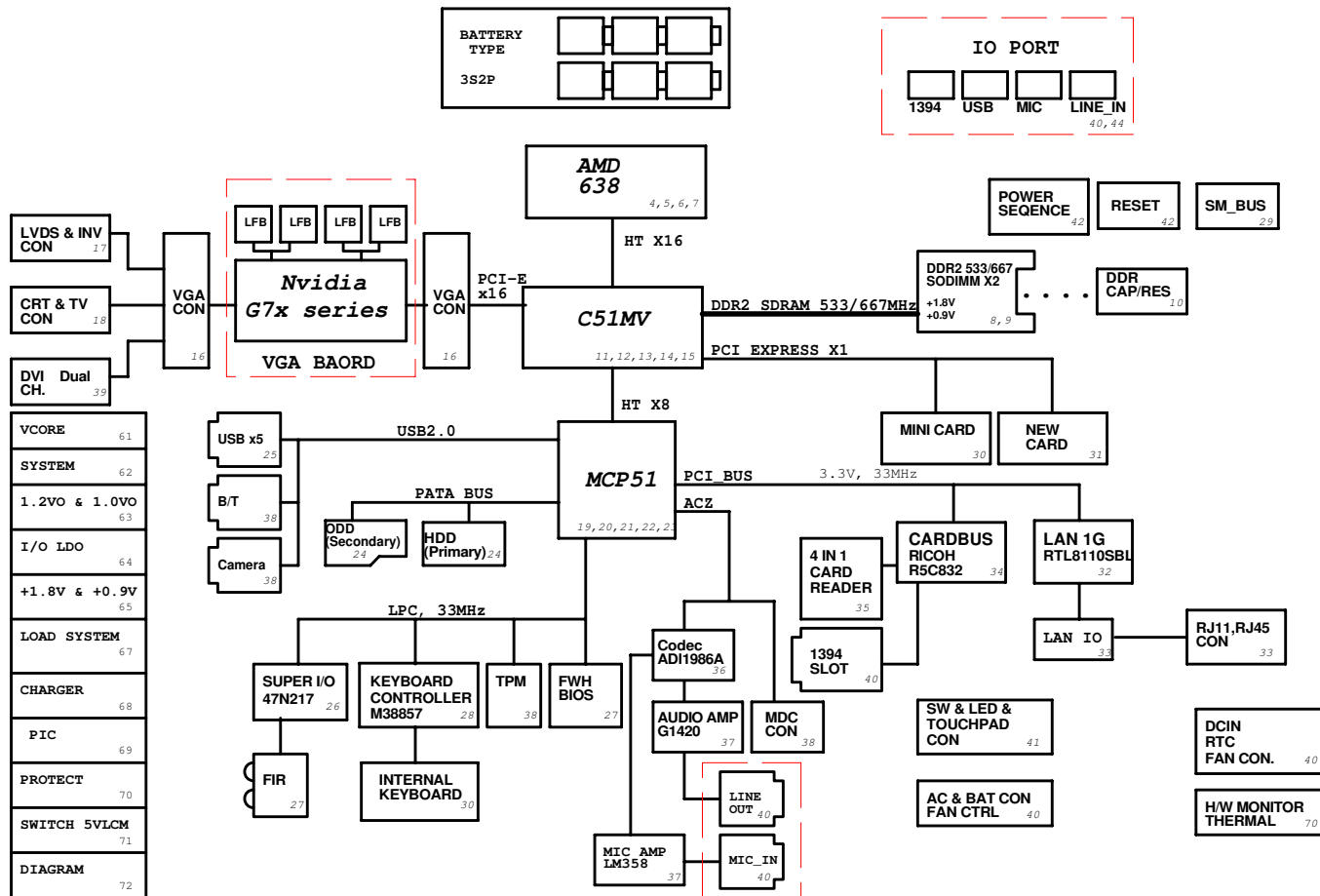


A8T/M SCHEMATIC R2.1


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	SYSTEM PAGE REF.		POWER PAGE REF.	
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5	AMD S1 CPU--CNTRL	62	POWER_SYSTEM	
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7	AMD S1 CPU--PWR/GND	64	POWER_I/O_LDO	
8	DDR2 SO-DIMM_0	65	POWER_I/O_DDR2	
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13	C51M--PCI-E	70	POWER_PROTECT	
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20	MCP51--PCI			
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22	MCP51--USB & HDA & GPIO			
23	MCP51--PWR/GND			
24	HDD & CD-ROM CONN			
25	USB PORTS			
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30	PCI-E--MINI CARD			
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35	PCI--4 IN1 CON			
36	AUDIO CODEC ALC660			
37	AUDIO AMP G1420			
38	MDC,B/T,TPM & DISCHG,HOLE			
39	DVI CONN			
40	ACIN, BAT, FAN, I/O PORT			
41	SW & LED & TP			
42	POWER-ON SEQUENCE			
43	HISTORY			
44	I/O PORT			

<Core Design>

A8T/M AMD S1/C51MV BLOCK DIAGRAM



<Core Design>

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		2.1	SHEET 2 OF 55		RELEASE DATE :	Albert Su

www.schematic-x.blogspot.com

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)


MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWR_LMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CABLE_DET)	+3VSUS
GPIO_[11:16]		(CPU_VID[0:5])	+3VSUS
GPIO_17		(LID#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDIN0_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	SIO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(RI#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

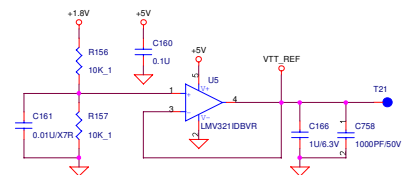
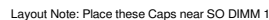
MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

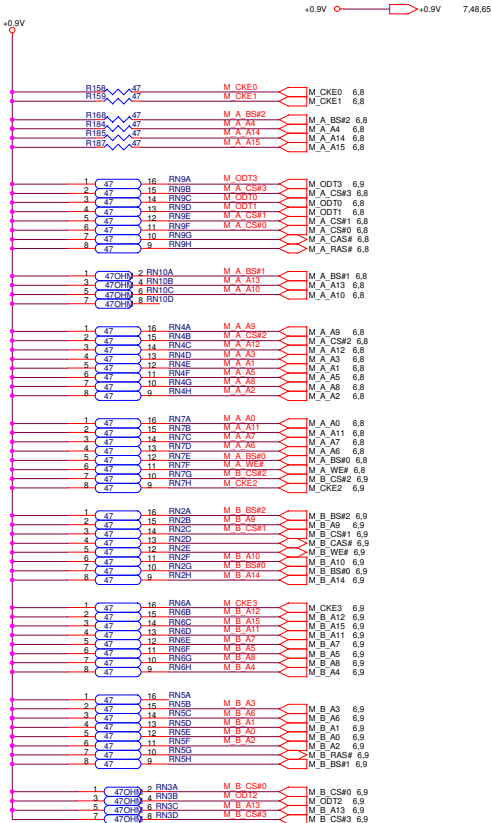
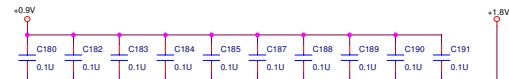
47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

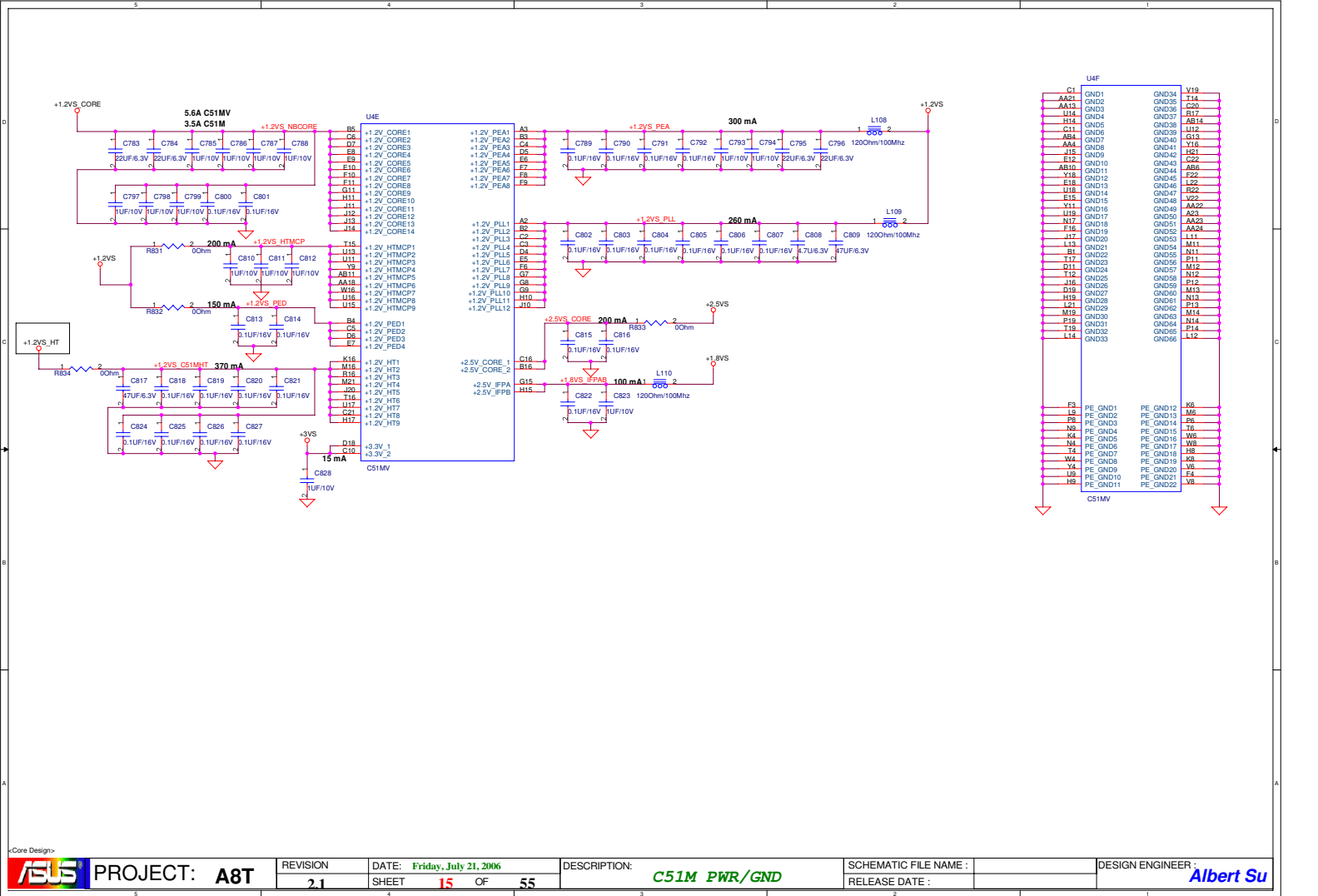
M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

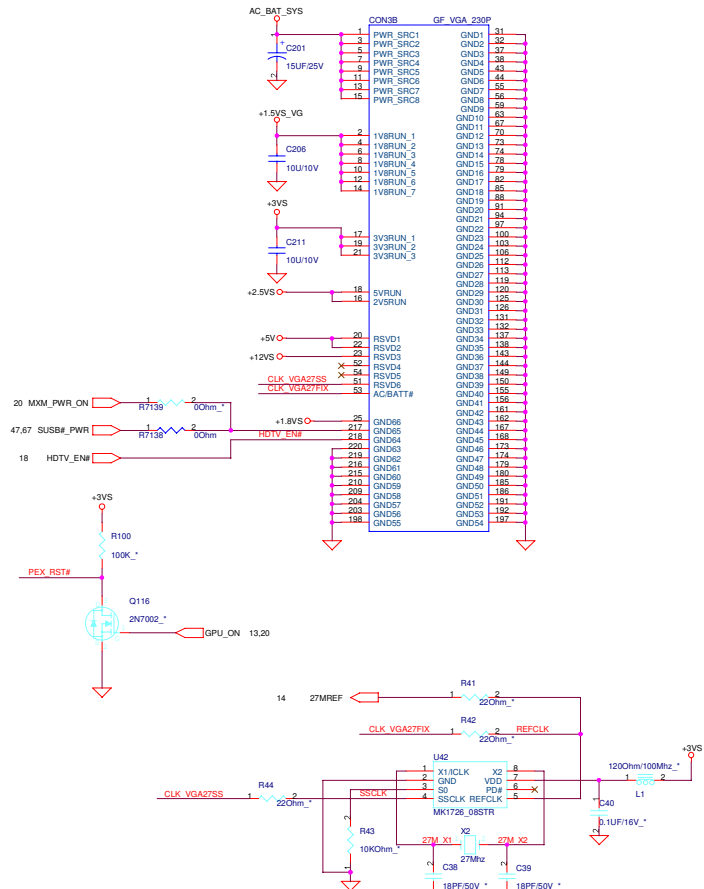
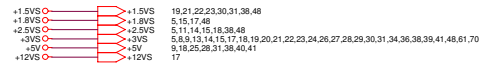
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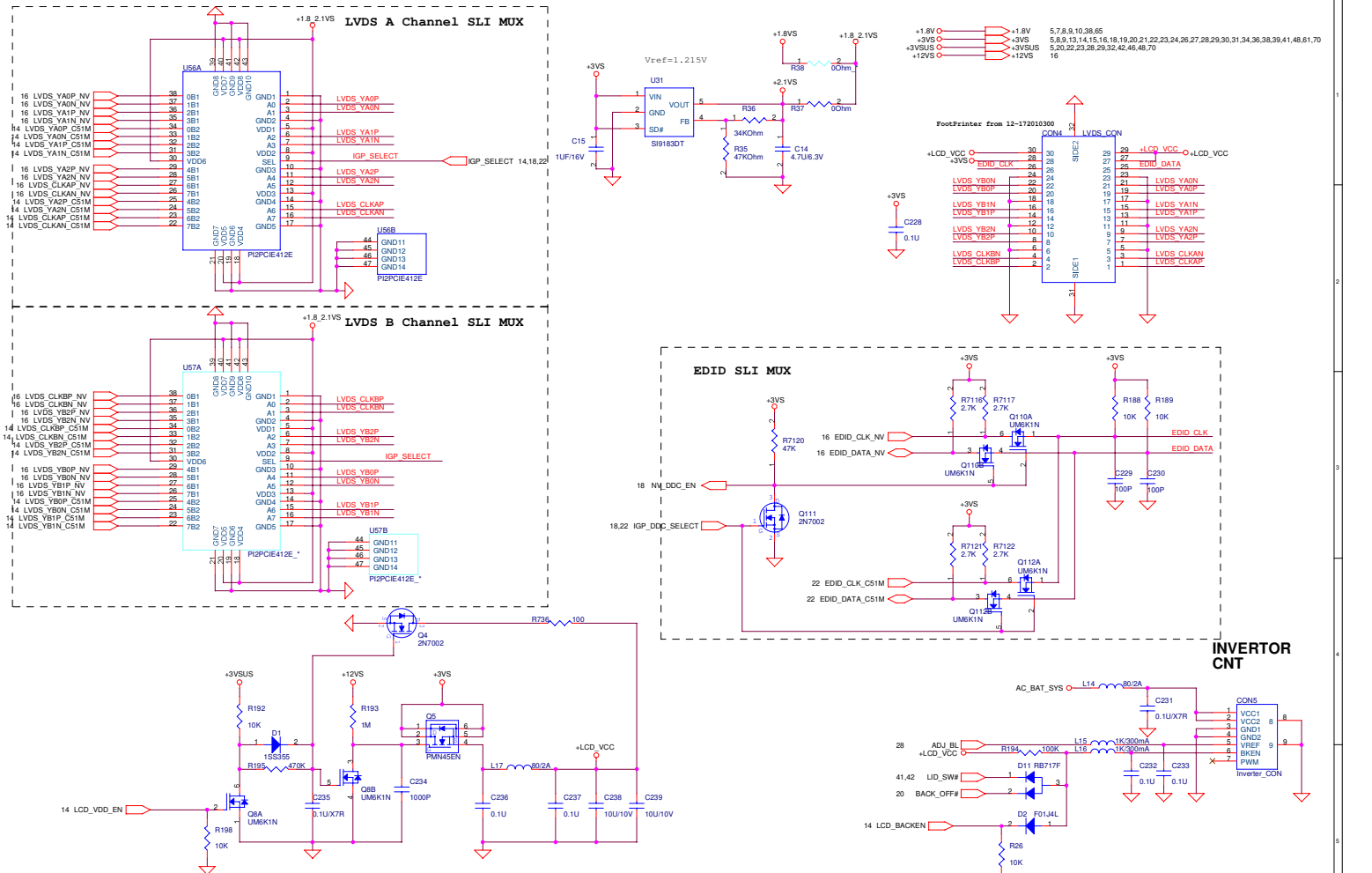
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		2.1	SHEET 3 OF 55		RELEASE DATE :	

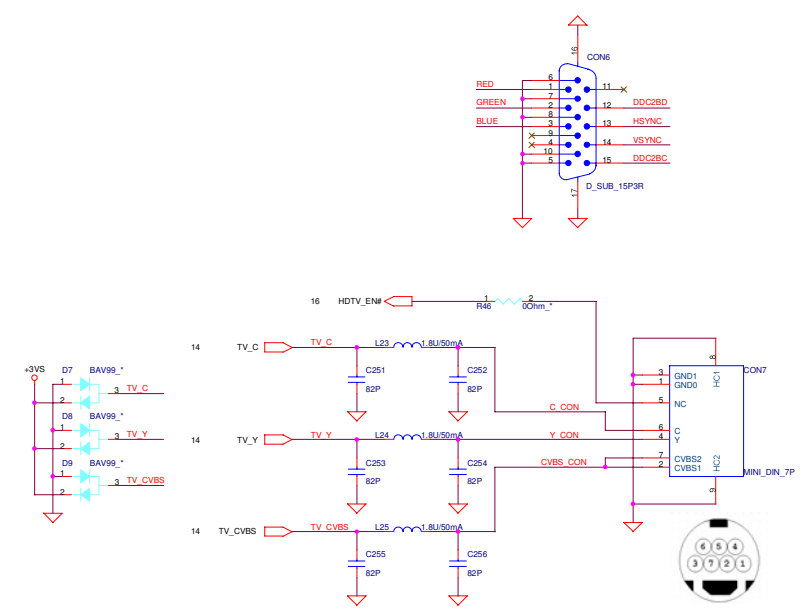
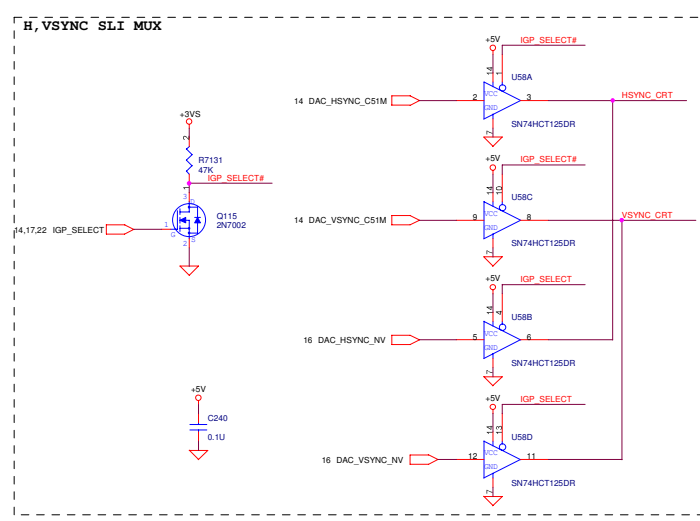
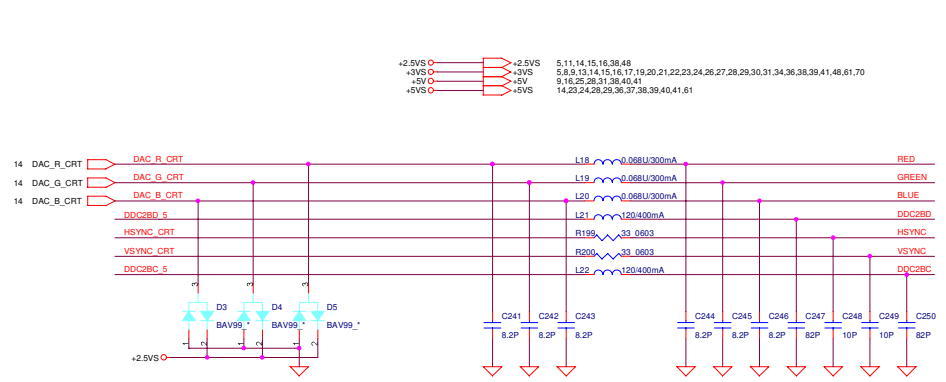
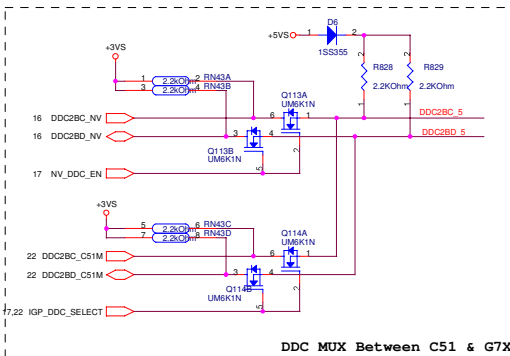


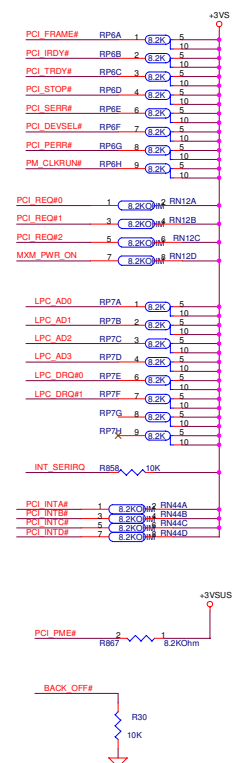


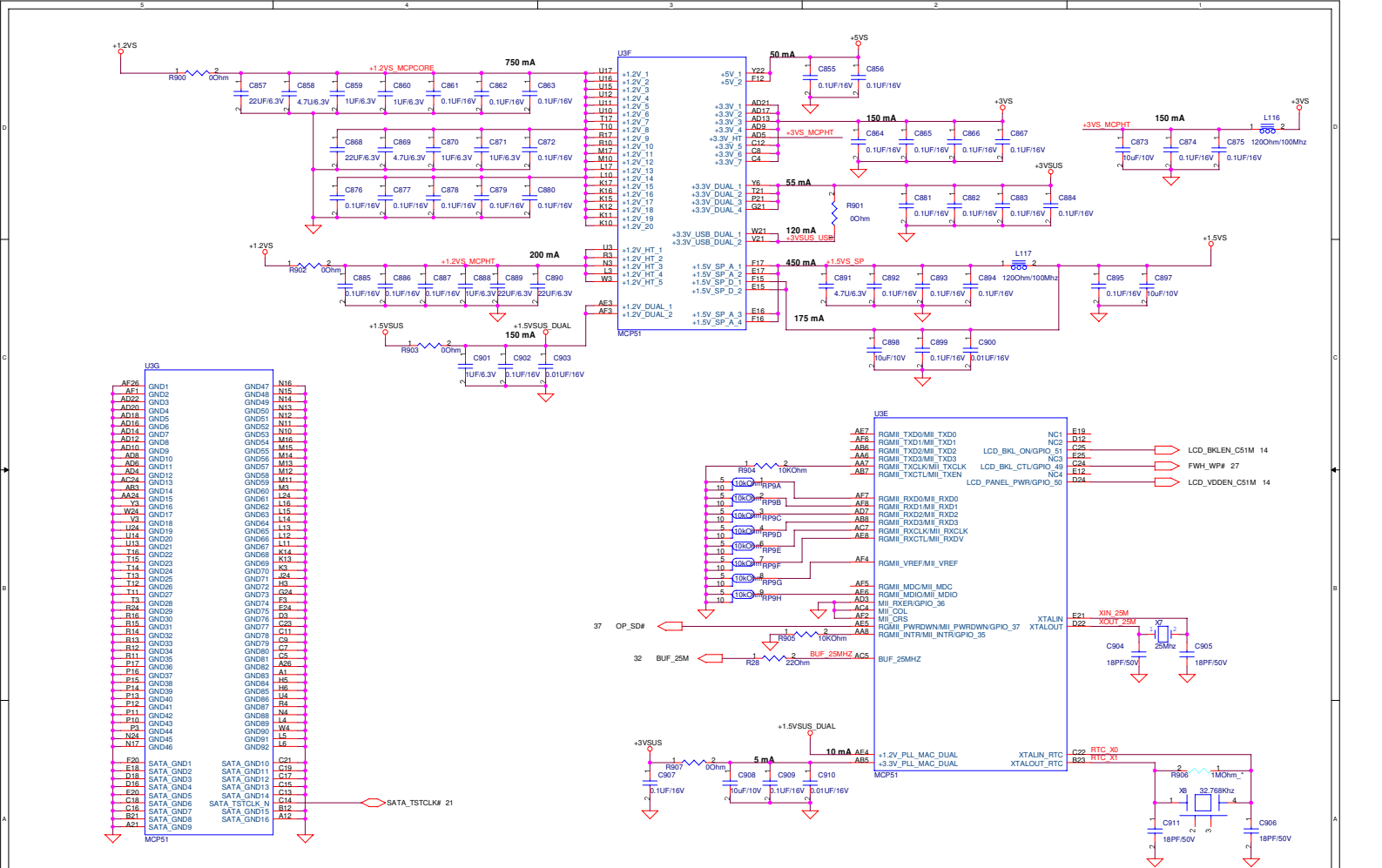






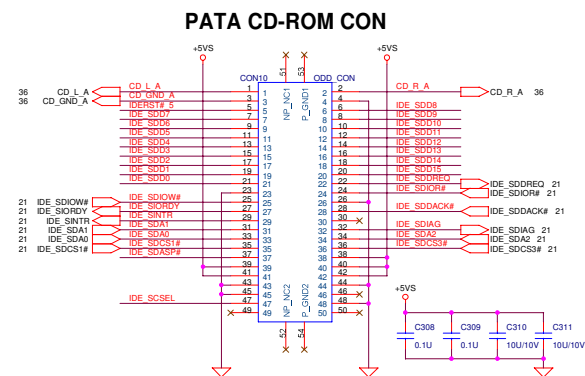
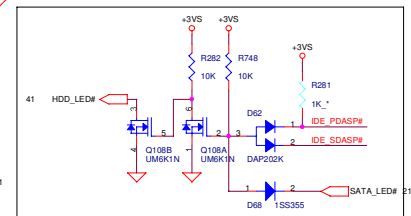


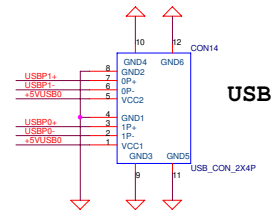
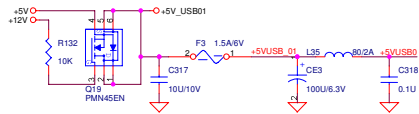
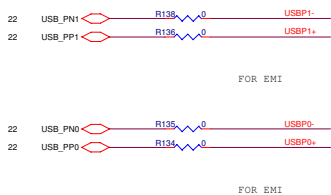
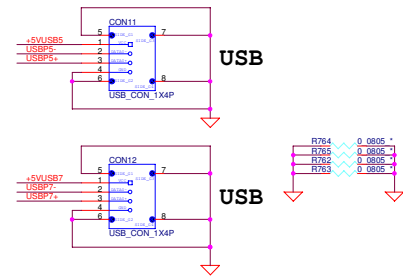
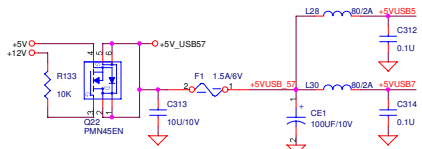
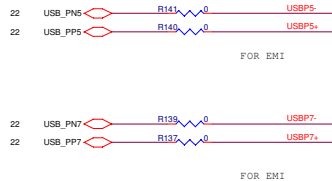




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	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME: 	DESIGN ENGINEER: Albert Su
		SHEET 23 OF 55			RELEASE DATE: 	

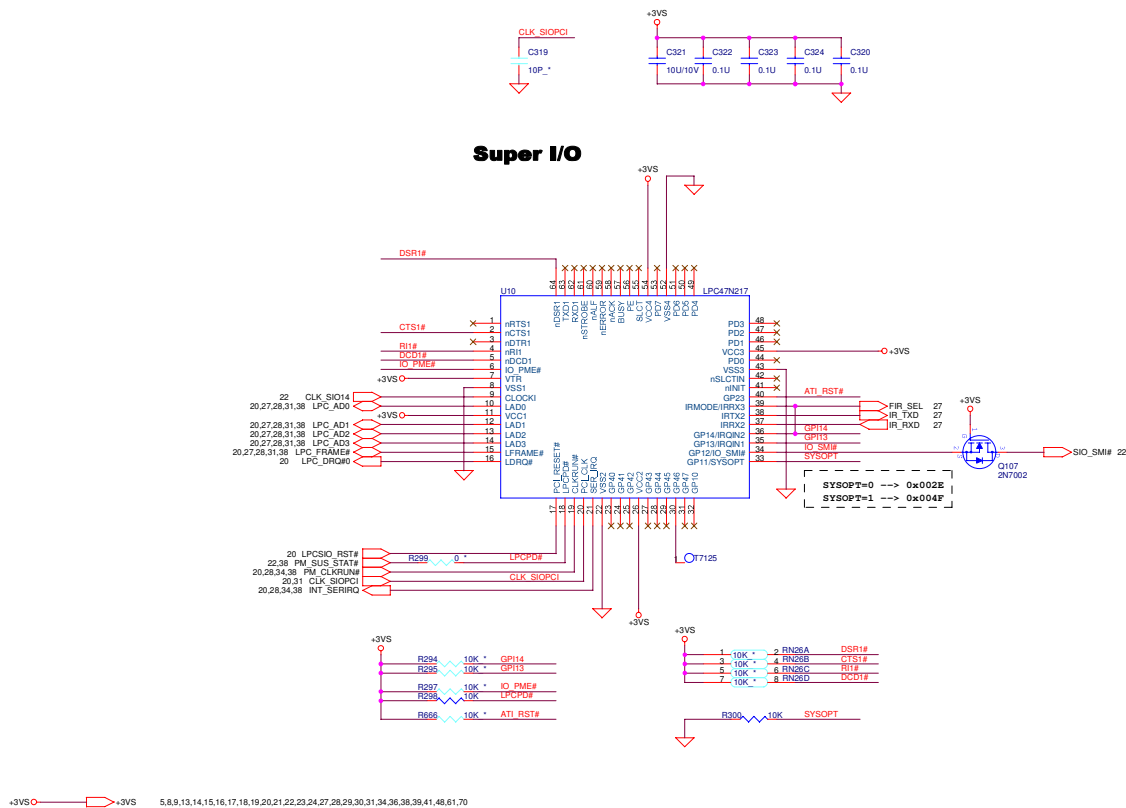


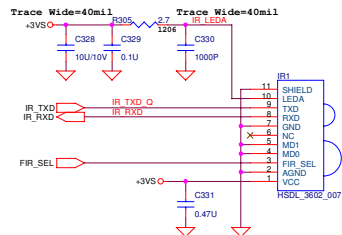


+5V +5V 9,16,18,28,31,38,40,41

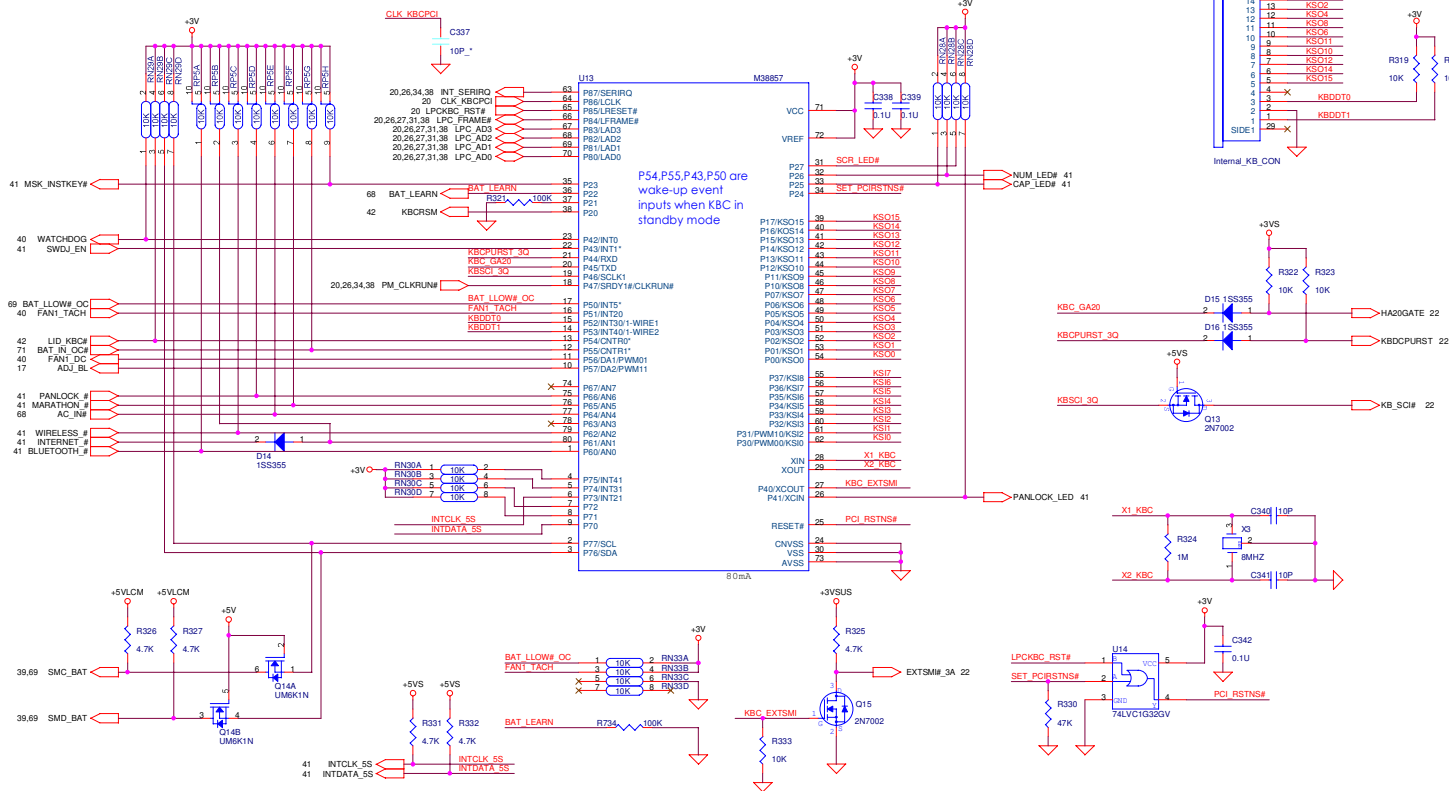
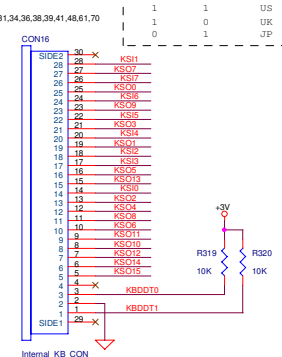
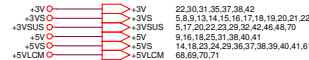
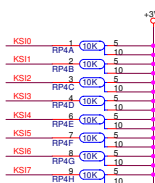
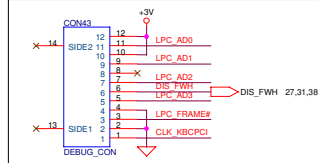
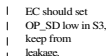
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	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		2.1	SHEET 25 OF 55		RELEASE DATE :		





DESIGN ENGINEER: **Albert Su**



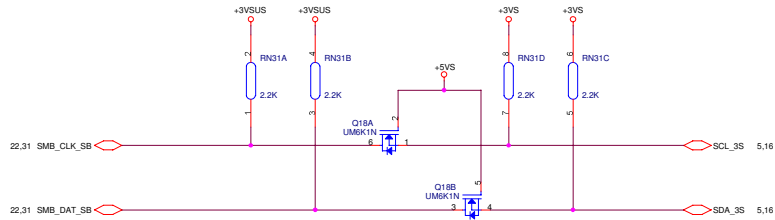
REVISION
21

DESCRIPTION:	KBC 38857
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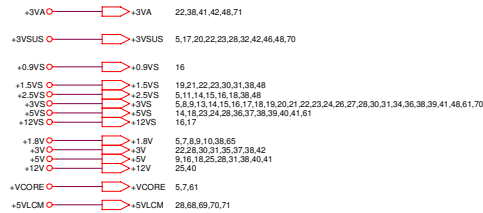
SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER : *Albert Su*

MCP51



Thermal Sensor,
TPM



<Core Design>



PROJECT: **A8T**

REVISION
2.1

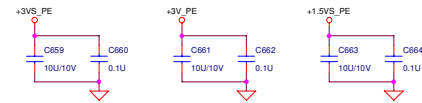
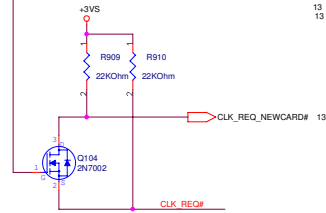
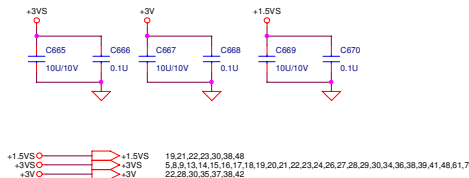
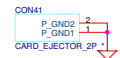
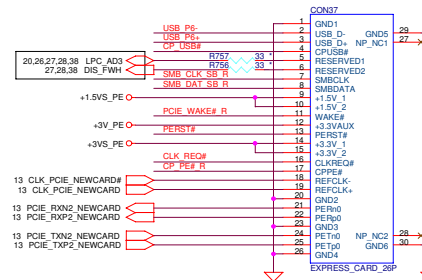
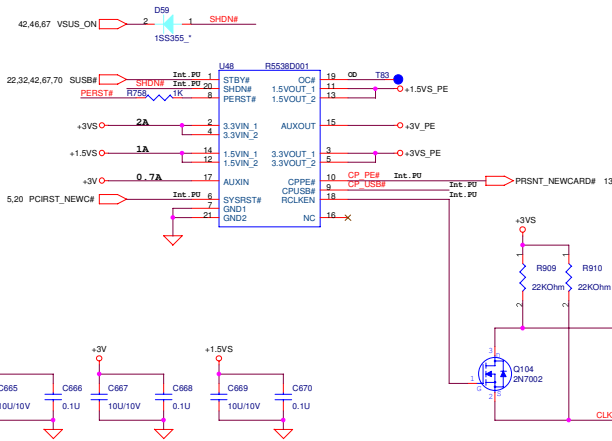
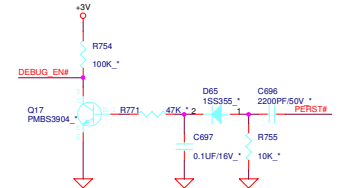
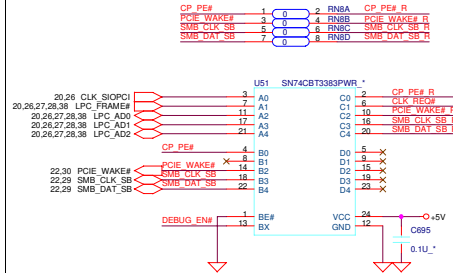
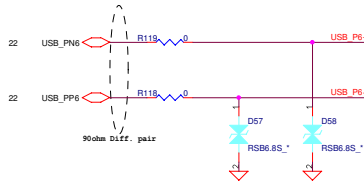
DATE: **Friday, July 21, 2006**
SHEET **29** OF **55**

DESCRIPTION:
SM BUS & POWER PORT

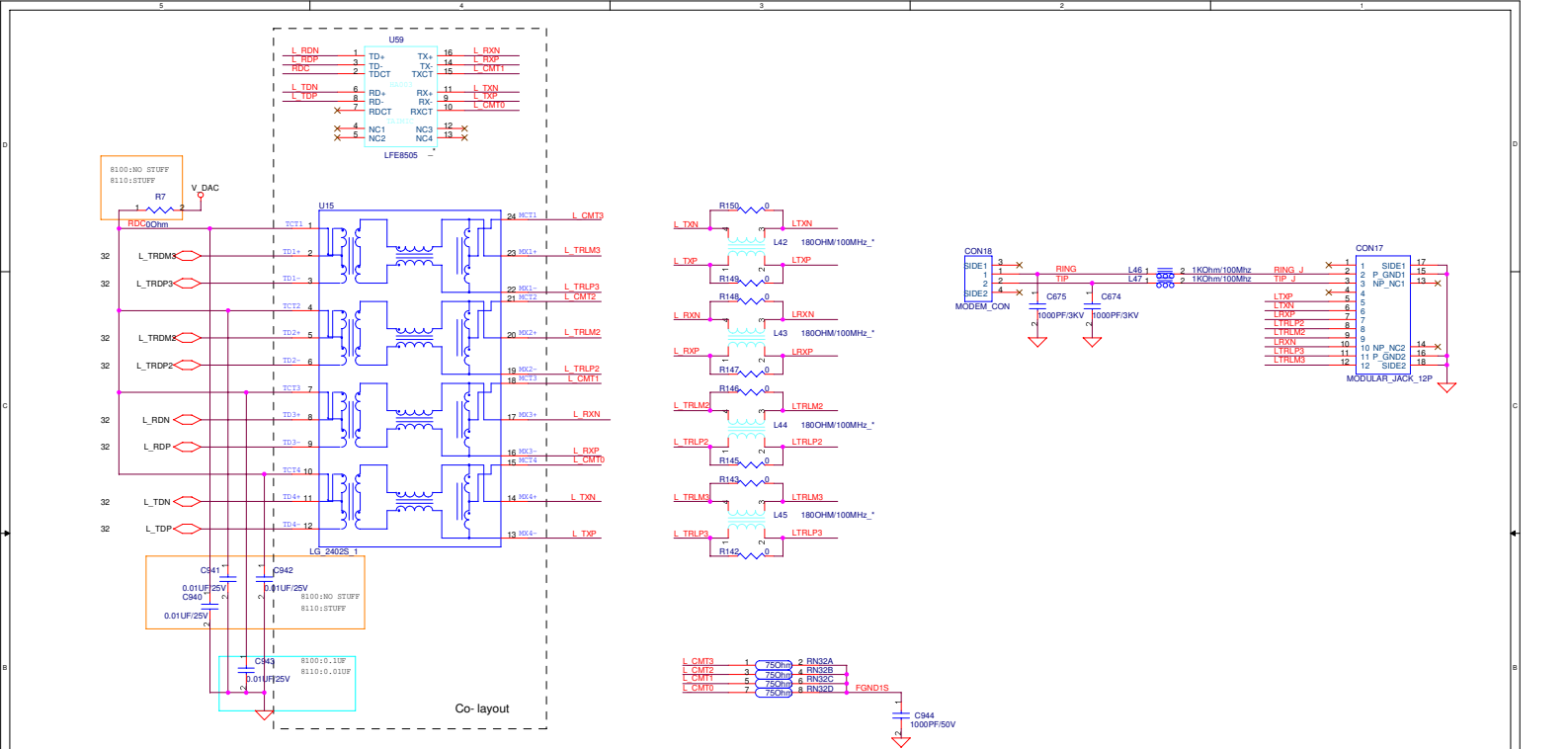
SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Albert Su



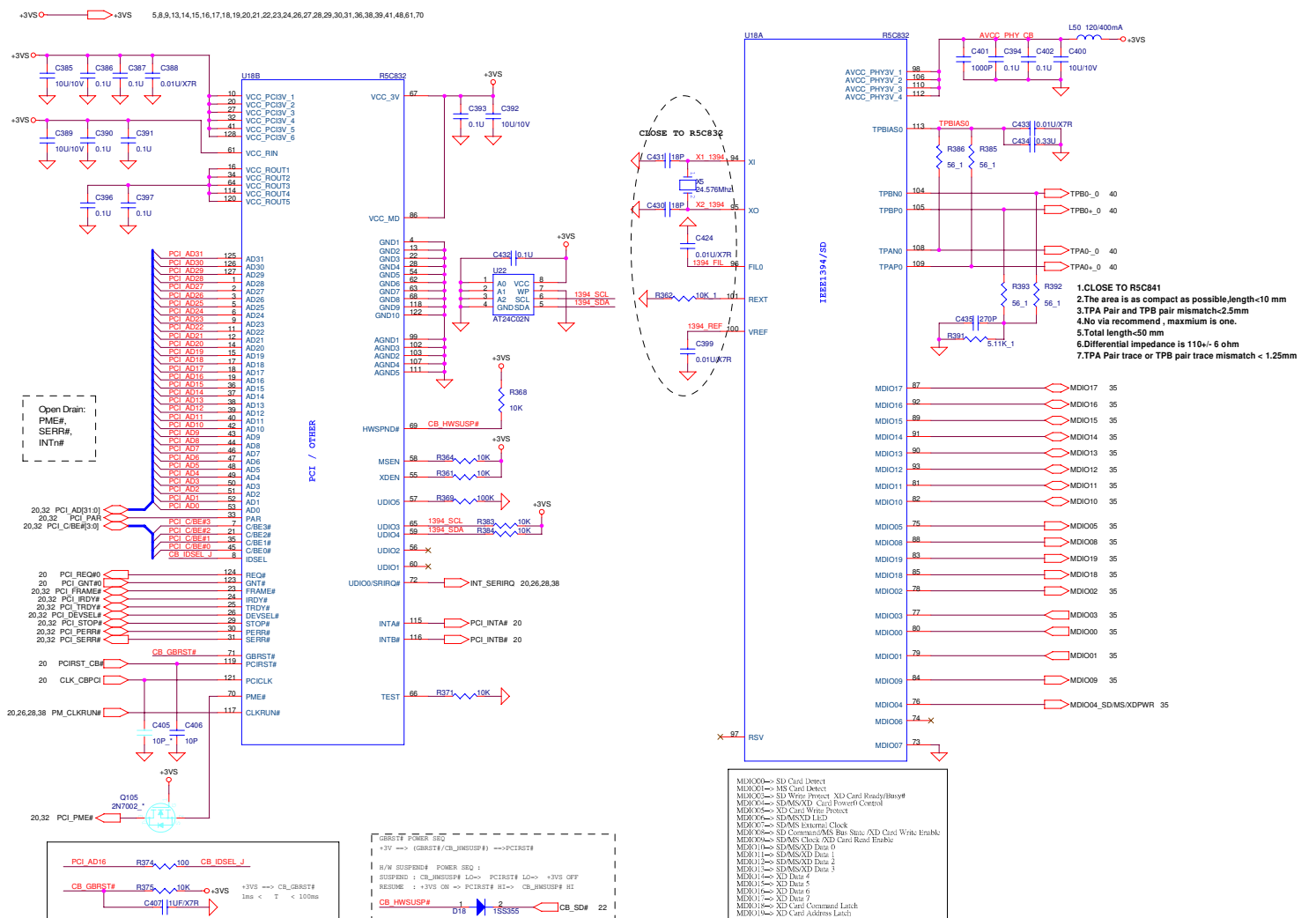


+1.5V O 19,21,22,30,38,48
+3V O 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,34,36,38,39,41,48,61,70
+3V O 22,28,30,35,37,38,42

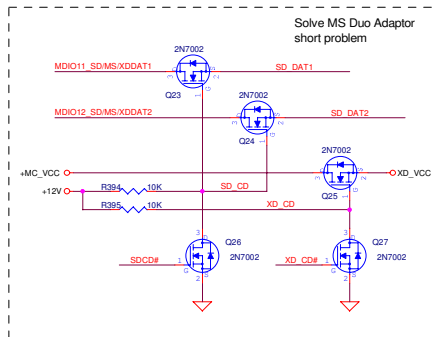
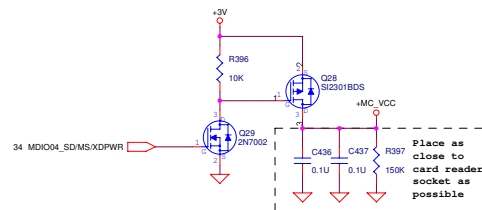
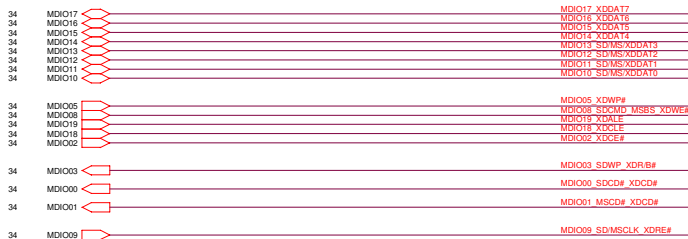


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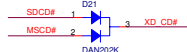
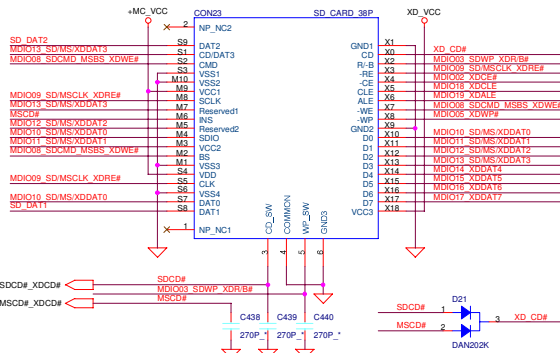
ASUS	PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006 SHEET 33 OF 55	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Albert Su
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1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5 mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110 +/- 6 ohm
7. TPA trace or TPB pair trace mismatch < 1.25 mm



+3V 22.28,30.31,37.38,42
+12V 25.37,40.67



<Core Design>



PROJECT: **A8T**

REVISION: **2.1**

DATE: **Friday, July 21, 2006**
SHEET **35** OF **55**

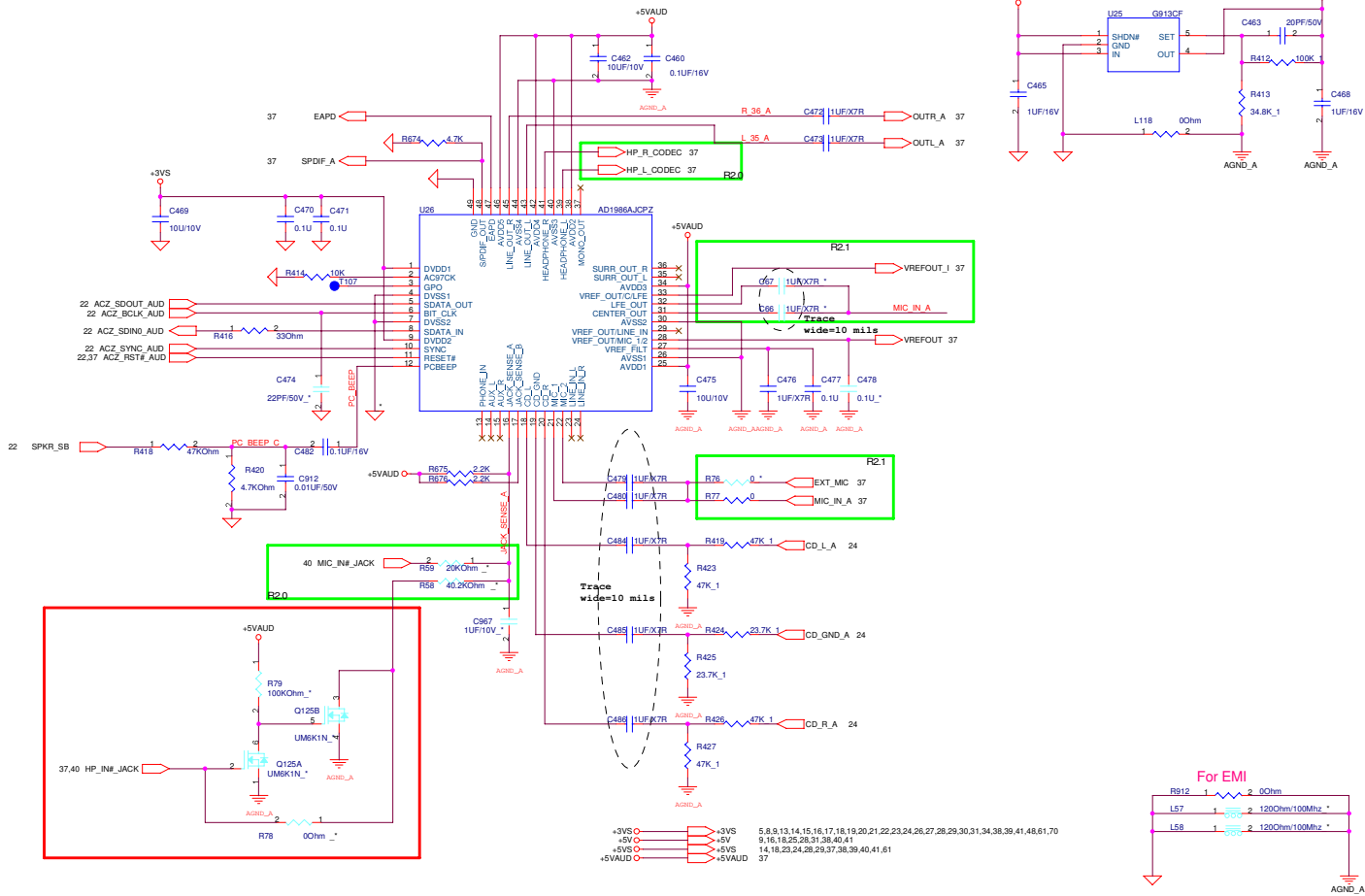
DESCRIPTION: **4 IN 1 CONN**

SCHEMATIC FILE NAME:

RELEASE DATE:

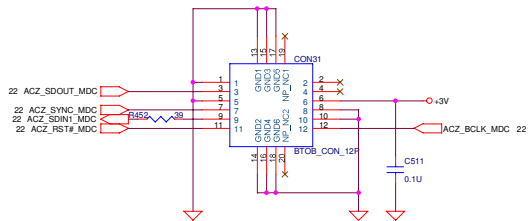
DESIGN ENGINEER:

Albert Su

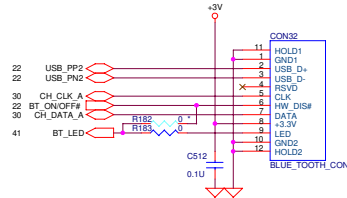


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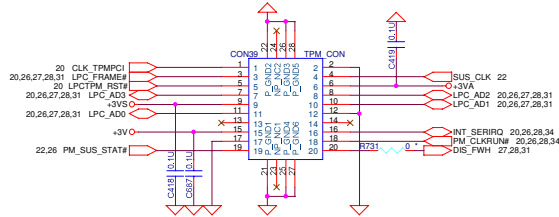
	PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006 SHEET 36 OF 55	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Albert Su
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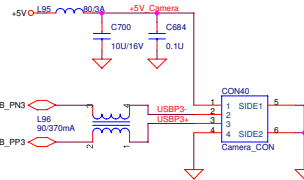
Azalia MDC MODEM CON



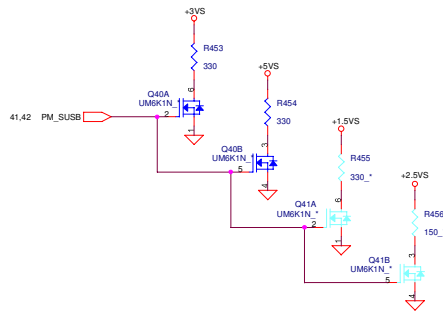
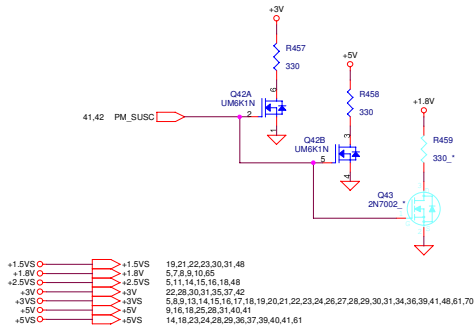
Bluetooth Module CON



TPM Module CON

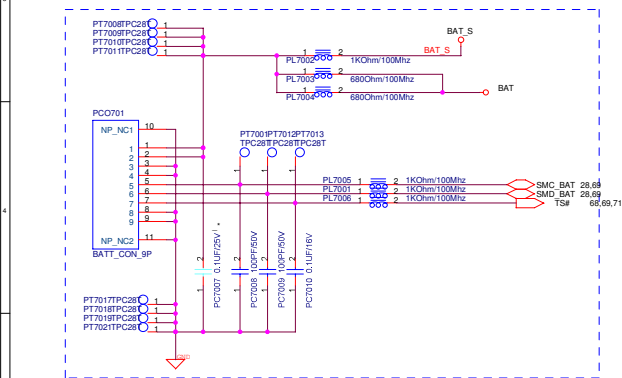


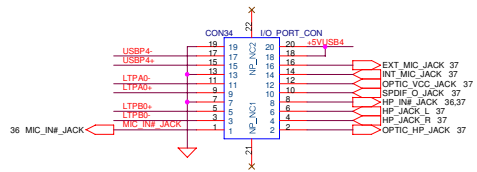
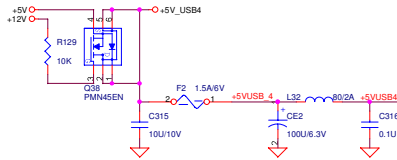
Camera Module CON



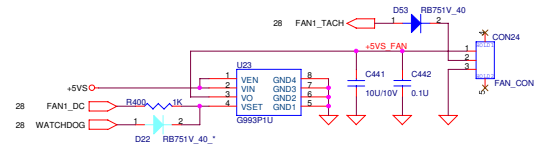
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	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MDC, B/T, TPM, Camera & DISCHG	SCHEMATIC FILE NAME: 	DESIGN ENGINEER: Albert Su
		SHEET 38 OF 55			RELEASE DATE: 	

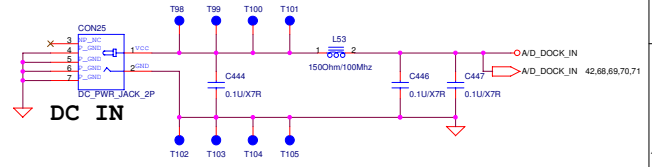




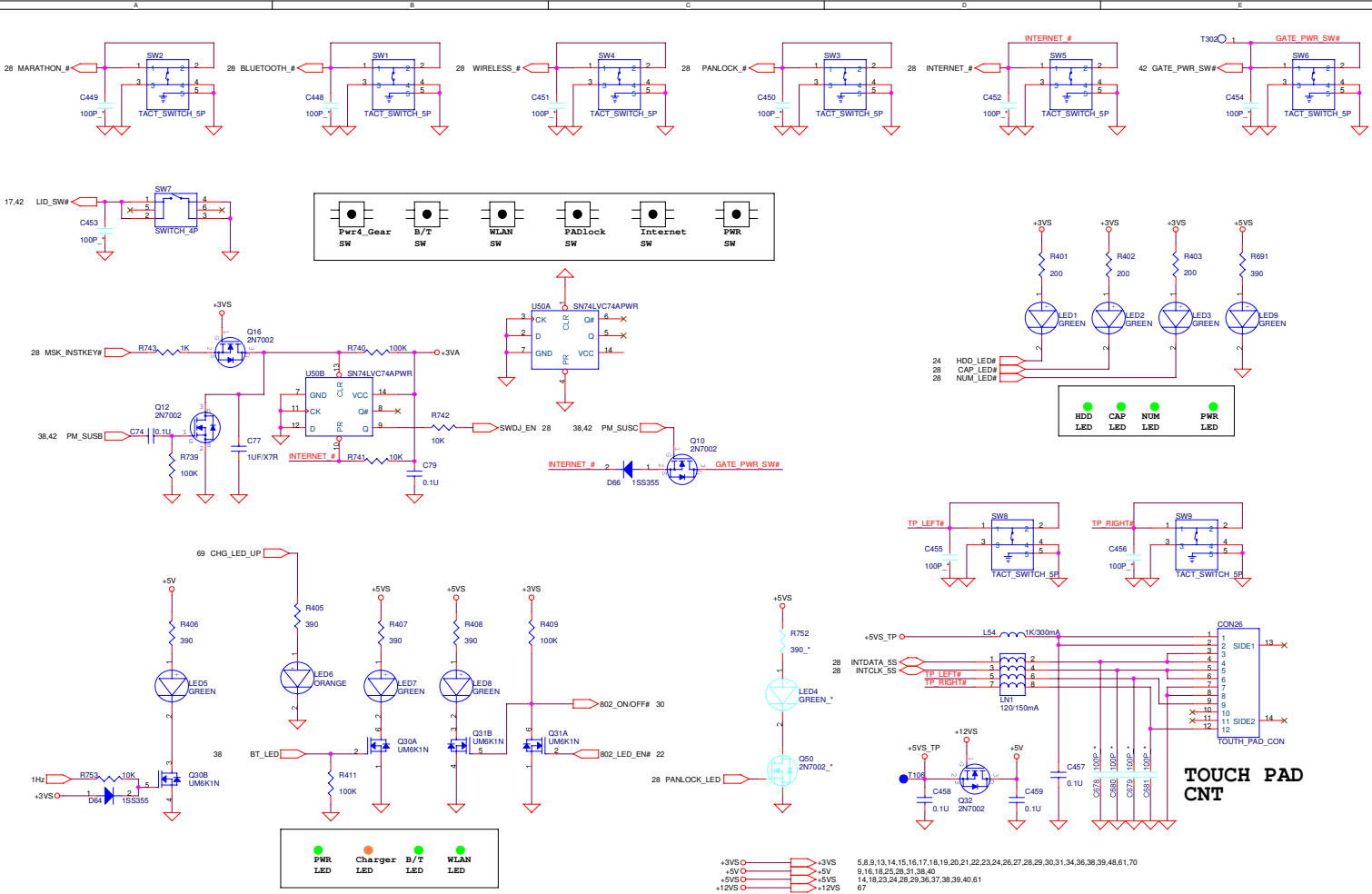
I/O PORT

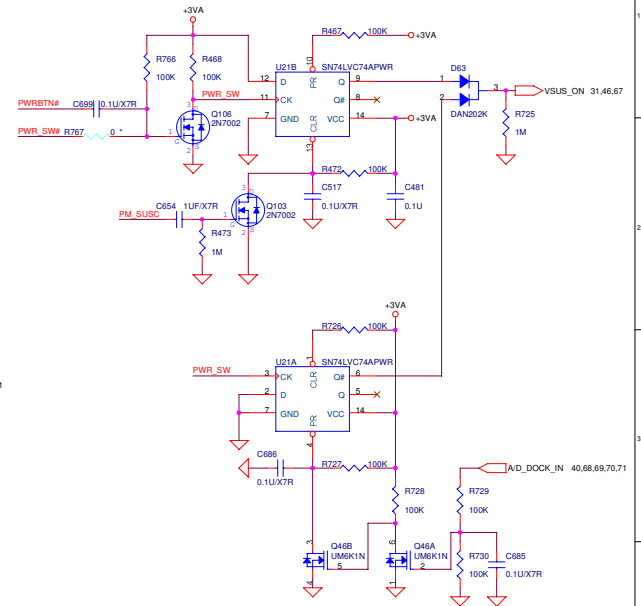
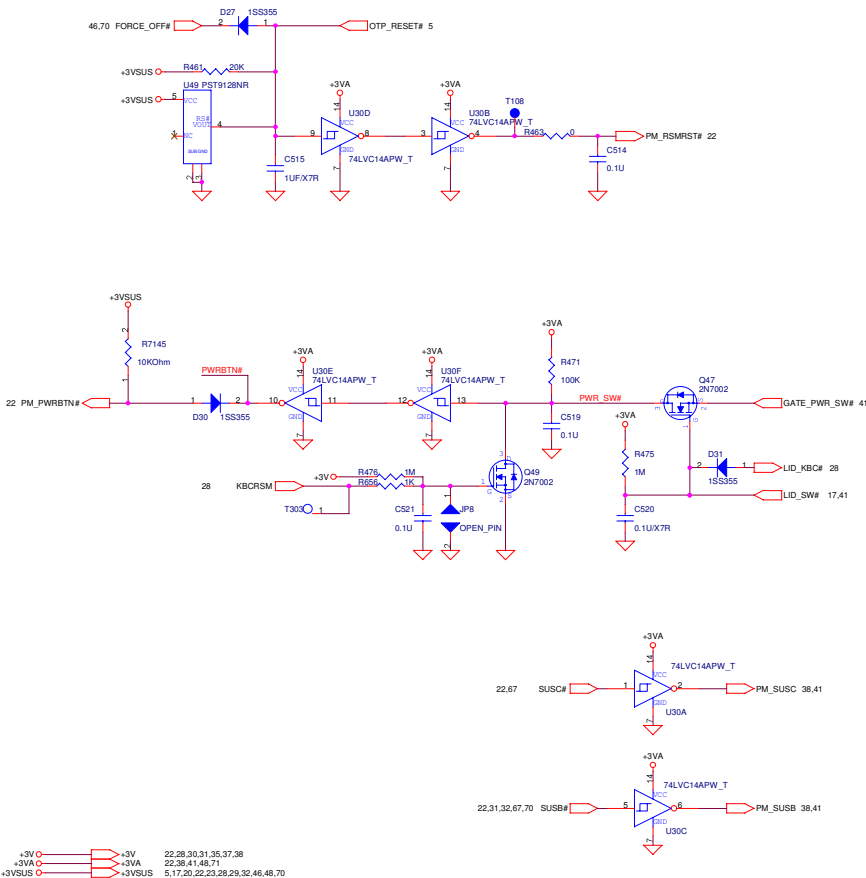


FAN CONTROL



ACIN_CONN





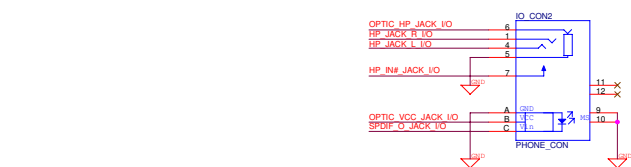
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ASUS	PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006 SHEET 42 OF 55	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Albert Su
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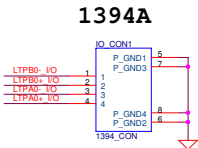
Revision History

Power:

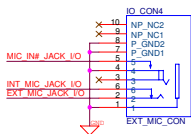
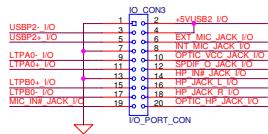
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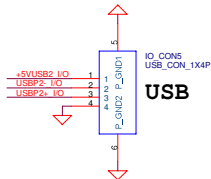
LINE_OUT
SPDIF



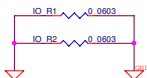
1394A



MIC



USB



<Core Design>



PROJECT: **A8T**

REVISION: **2.1**

DATE: **Friday, July 21, 2006**

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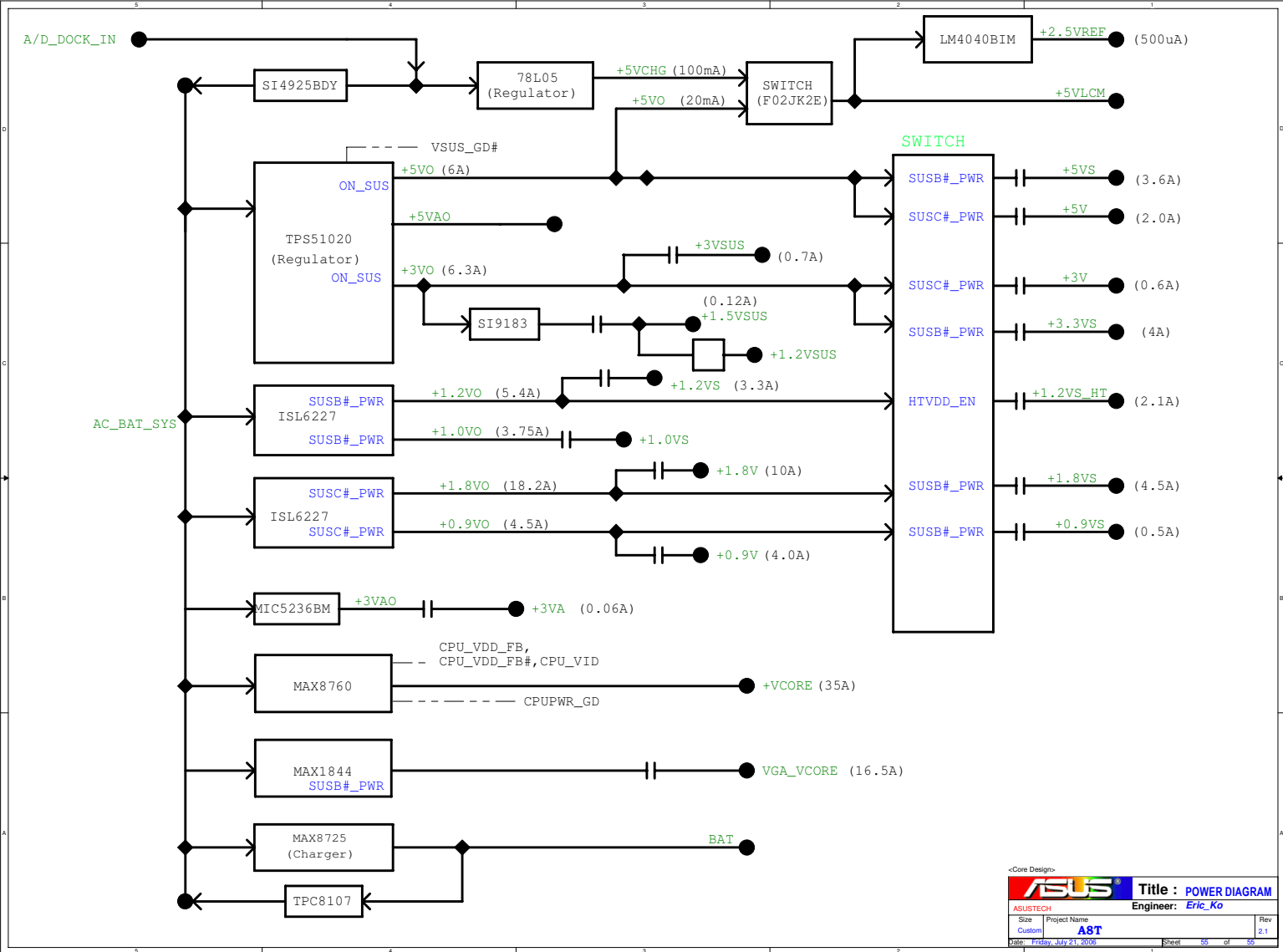
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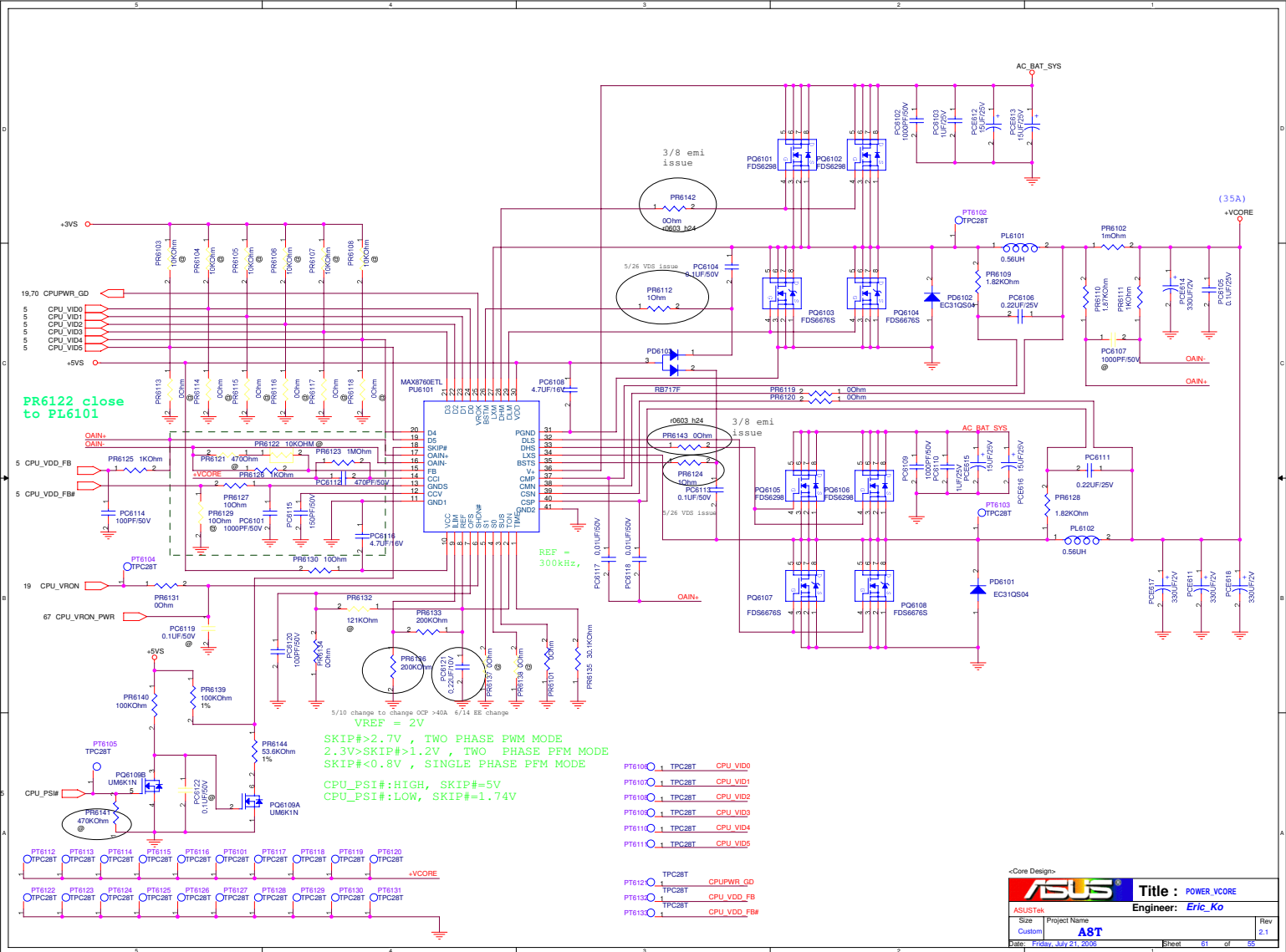
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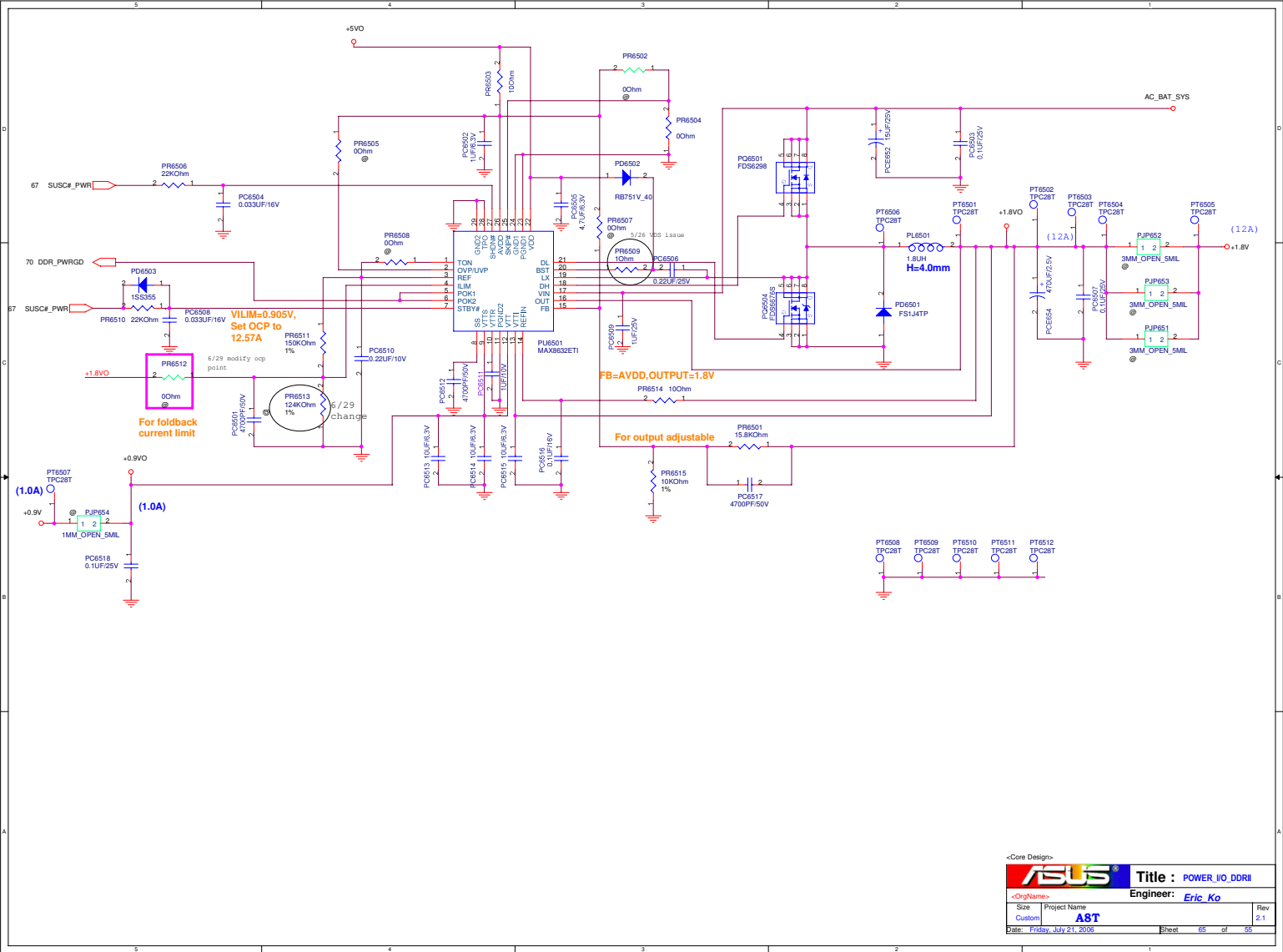
DESIGN ENGINEER :

Albert Su



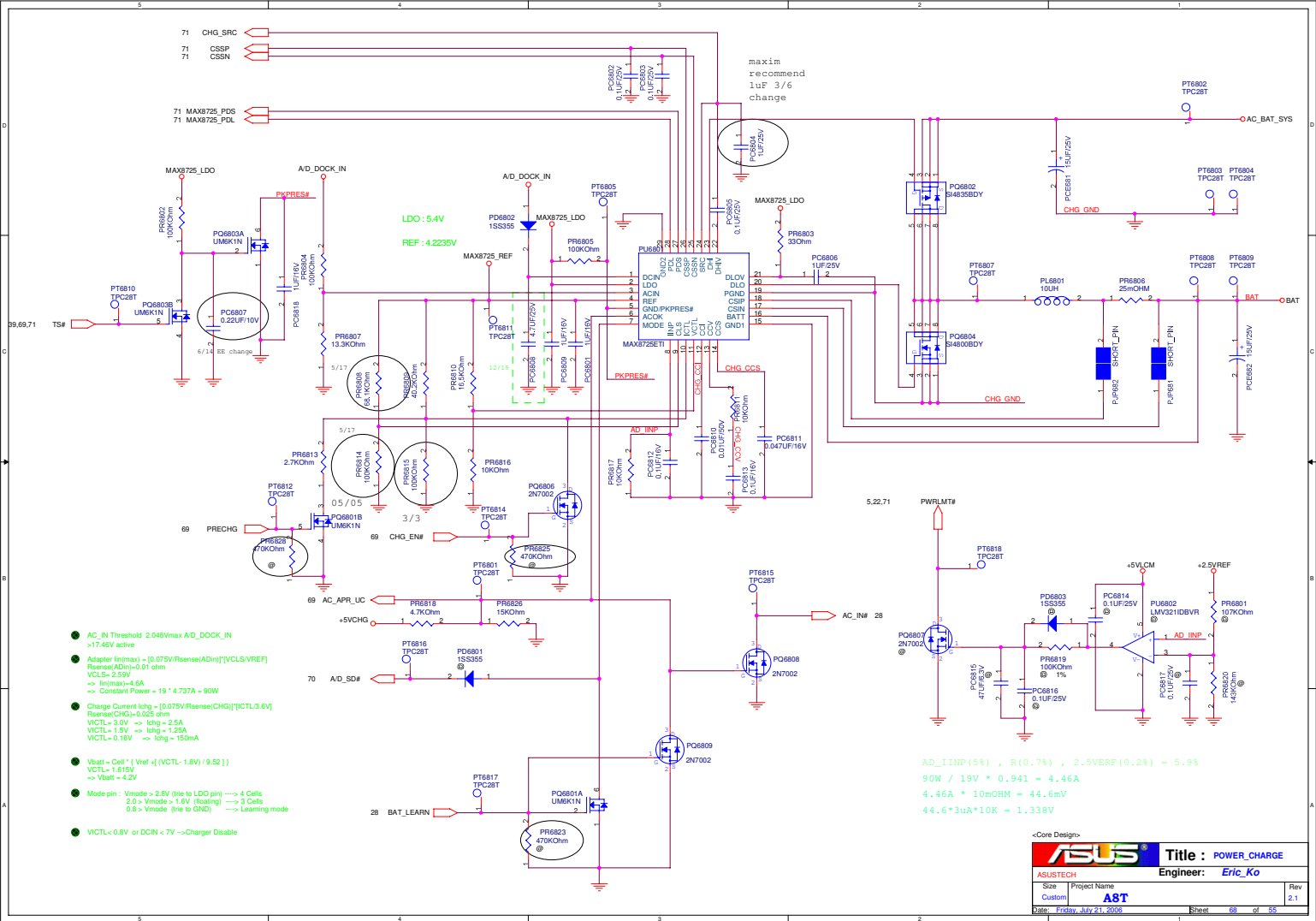






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		Title : POWER I/O DDRII	
<OrigName>		Engineer: Eric Ko	
Size	Project Name	Rev	
Custom	A8T	2.1	
Date: Friday, July 21, 2006		Sheet 65 of 95	



PIC16F54

